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14. ABSTRACT

Purpose: The purpose of this project is to create new sensor technologies and perform preliminary studies in an impact model of TBI for subsequent rapid transition to testing in blast TBI models with future funding opportunities. The hypothesis is that measurement of intracranial pressure transients in an impact model of traumatic brain injury will provide valuable data about sensor performance within a biological system that will be directly applicable to subsequent transition into blast TBI animal models.
Scope: Miniaturized, state-of-the-art pressure/temperature sensors will be engineered and fabricated to measure the immediate increases in intracranial pressure (ICP) combined with longer-term measurements of biological ICP and intracranial temperature during experimental TBI. Experiments will measure of acute transmission of pressure waves through the brain, longer-term changes in biological ICP, and intracranial temperature.
Major Findings: Currently, the first lot of pre-etched silicon-on-insulator wafers have been built. Those wafers are now entering processing to define the ion implants and metal contacts to create the strain-sensitive circuit of the device. We are performing failure testing of the diced and etched wafers on in a custom designed bending apparatus.

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Introduction:

The major objective of this research effort was to create new sensing technologies and perform preliminary studies prior to rapid transition to testing in blast TBI models. This project proposed to use miniaturized, state-of-the-art pressure/temperature sensors engineered at LLNL to measure the immediate increases in ICP combined with longer-term measurements of biological ICP and intracranial temperature. The experience gathered from this seed proposal provided valuable data on sensor placement, long-term brain tissue responses to implanted sensors, and sensor capability of dual measurement of biologic ICP and impact pressure transients that will be directly applicable to subsequent transition into blast TBI animal models.

Body:

Year 3 funding (no-cost extension):
Task 3: (optional year effort): To implement multi-modality micro sensors (evaluated in Funding year 1) in a large animal model of blast TBI.

In our final report at the conclusion of our year 1 funding we stated that:

> "A shortcoming of the modified sensors was the inability to measure very low pressures associated with biological ICP from brain edema (less than 1 psi). Engineering calculations indicate that a thinner sensor diaphragm will make such small pressure measurements feasible without compromising high pressure measurements associated with blast TBI. The third generation sensors are planned to be designed and fabricated for the option year of this project."

Dr. Kotovsky at LLNL has continued to improve the sensors through re-engineering the previous sensor and designing a new 3rd generation sensor to address the shortcomings described above.

Currently, several sensor development activities are underway. The results of these efforts will yield the first wafer-scale, absolute pressure sensor in a similar ultra-thin form factor as the contact stress sensor. These sensors are under development to meet the specific needs of the TBI study. Their thinness and unobtrusive packaging allow for ready insertion to numerous intracranial sites. To produce these sensors at a wafer scale, a new MEMS fabrication approach has been developed and is currently being executed for the first time. For absolute pressure sensing, the contact stress sensor must be modified to create a reference cavity; a trapped volume of gas that is hermetically sealed within the device. The new process pre-defines the pressure sensor's reference cavity within the Silicon-on-insulator (SOI) wafer. The pre-definition provides a variety of advantages to the overall process:

- The cavity definition requires a plasma etch that is a challenging operation to perform on a thinned substrate, performing this etch at the start of the SOI build pushes the process to a thick-wafer operation simplifying the processing significantly

- Producing the reference cavity requires a hermetic seal that requires a high temperature operation that is difficult to perform later in the process once metals are on the substrate
- Pushing the cavity formation to the start of the process reduces yield risk by placing the most difficult process at the start of the fabrication (least substrate added-value)
- Pre-definition of the cavity paves the way for no backside processing of thinned substrate increasing the overall yield of the substrates
- Etching of the cavities prior to metallization keeps the etching process CMOS clean
- Commercialization of the sensor is aided by this process as use of CMOS-clean commercial foundries will not be restricted

In parallel with the wafer-scale absolute sensor process, several other important changes are underway in parallel. The new process includes a CMOS-clean metal stack throughout the cleanroom processing. Similar to the non-metal etching mentioned above, maintenance of CMOS-clean metals allows any foundry to build the substrates. A major difficulty in finding commercial foundries to perform the sensor process was locating MEMS-specific foundries willing to work with our non-CMOS metals used to date. LLNL's clean room is not restricted by these metals but most external foundries are. A goal of this project is to identify and execute the process at an external foundry. This is being pursued for two reasons, 1) there is a significant cost and time savings by performing this work externally and 2) use of an external foundry allows ready transfer of the technology to the commercial sector as LLNL cannot act as a commercial foundry. The CMOS-clean metals require modification of the solder joint with the package. We are accomplishing the modification by use of a solder-ball bumping process at a commercial vendor. Solder bumping is an industry standard and an established process. Adaptation of this process has some risk but if successful, will greatly reduce the packaging cost of the finished part. The cost savings is the result of application of the solder to the wafer scale (1000's of sensors at a time) vs. the package scale (10's of sensors at a time).

The solder bumping testing began with identification of the correct solder ball size to produce the needed solder bump height after reflow. Calculations identified the expected bump height based on the solder ball volume. The exact parameters were established by testing the designed solder ball volume on the defined bond-pad size (the bond-pad size dictates the solder reflow wetting area and thus the finished solder height). The designed pad size was bracketed above and below by 20 microns. The test run showed a robust outcome with all three pad sizes, each forming excellent solder joints with the test packages. Based on this study, a metal bond pad size was chosen and designed into the sensor photolithography masks.

Additional work is underway to investigate singulation of the silicon MEMS die by a cutting process in lieu of an etching process. With the pre-defined recesses in the SOI wafer, a backside process for the recess definition after wafer thinning is not required. The other backside process used up to this time is plasma etch to singulate the die. If a substitute for this process can be identified, no backside processing will be required of the wafers. This represents an enormous cost savings and improved yield. Again, it allows the process to move forward in CMOS clean facilities. The obvious choice for singulation is a wafer saw process. We are in the midst of cutting die now to confirm that the edge roughness does not pose a fracture risk to the thinned die. As these sensors are exceptionally thin (~65 microns), their strength is a concern. A rough sidewall may facilitate chip cracking and device failure. We are sending diced samples and etched samples to a private company to perform failure testing on in a custom bending apparatus we are designing together. Development of this process will continue to identify a working singulation technique if issues arrive. Alternatives are laser dicing, sidewall polishing or reverting back to plasma etching.

Key Research Accomplishments:

- Currently, the first lot of pre-etched SOI wafers have been built.
- Those wafers are now entering processing to define the ion implants and metal contacts to create the strain-sensitive circuit of the device.

Reportable Outcomes:

Nothing to report.

Conclusion:

In the remaining time of our current no-cost extension, we plan to have the newly designed 3rd generation sensor chips fabricated and in-hand and then packaged (encased) for in vivo animal use. We will then proceed to test the prototypes in the engineering laboratory prior to moving to our in vivo rat TBI model for practical testing. Specifically, the 3rd generation sensors will incorporate modifications to produce greater accuracy and reliability in measurements of biological ICP. We also plan to further refine the sensors into a smaller overall package and to design and implement a more user-friendly connection between the sensor and the recording instruments in order to make a smooth transition into making measurement in a blast TBI model later on in the project.

We expect initial results from all the work described above within the next several months. Design iteration will ensue as necessary. We intend to continue working with a private company interested in the technology who may become a commercial outlet for general use of the sensors for TBI and potentially other studies. We look forward to bringing the sensor to commercialized success.

References:

None

Appendices:

None